Title: Patterning and Characterization Engineer

Report to: Chief Technology Officer (CTO) and Senior Process Integration/Characterization Engineer

Locations: Changzhou and Suzhou, Jiangsu Province

Salary: Negotiable, depending on qualifications and experience

Job type: Full time, Permanent

Job description:

Under the direction of the CTO and the senior process integration/characterization engineer, the patterning and characterization engineer is responsible for the processing and characterization of prototype wafers for new technology programs and next generation projects, including performing patterning thin films into functioning nano/micro-devices, conducting failure analysis on prototype wafers and recommending corrective action.

Key responsibilities:

- Develops and delivers patterning processes for successful new devices
- Conducts failure analysis on newly developed processes and recommends corrective action if necessary
- Participates in characterization or integration projects of various scope and complexity; ensures they are completed within the established timeframe
- Reviews and analyses wafer level characterization data
- Performs wafer level process characterization on Crossbar structure devices using Focused Ion Beam (FIB)/SEM tool to identify defects and recommends corrective action
- Designs and conducts experiments to verify process robustness; analyses data and reports findings
- Analyses data using JMP, MS Visual Basic, or similar software application to determine the root cause of process variations; develops charts or reports and presents findings before groups or teams
- Collaborates with other team members, managers, or departments
- Adheres to all safety policies and procedures as required
- Performs other duties of a similar nature or level

Job requirements:

Minimum qualifications:

- Master's degree in Electrical Engineering, Materials Science, or Physics and/or equivalent relevant experience; PhD degree preferred
- 3 years of hands-on experience working in the process integration or characterization in a semiconductor industry/university in a manufacturing or process engineering role
- Hands-on experience using various different thin film patterning techniques
- Proficient in the use of Microsoft Office Applications

Knowledge, skills and abilities:

- Strong knowledge of process integration and characterization principles, practices, and techniques – with a focus on micro/nano patterning of metal, and metal oxide devices
- Knowledge of magnetic memory technology/ReRAM/PCRAM technology (not essential but a plus) – clean room processing and characterization.
- Knowledge and ability to use Microsoft Office applications to create spreadsheets, Word documents, and presentations in Chinese and English (not essential but a plus)
- Able to design experiments, analyse results, and recommend corrective action
- Able to communicate effectively, both verbally and in writing, with all levels of contractors, consultants, employees, and management
- Able to work productively and collaboratively with all levels of employees and management
- Able to comply with all safety policies and procedures
- Able to use critical thinking to resolve issues, conduct root cause analysis, and make recommendations for process improvements
- Demonstrated analytical skills
- Demonstrated organizational and time management skills
- Demonstrated problem-solving and trouble shooting skills

- Flexible and be able to prioritize tasks

Working conditions:

Patterning and characterization engineer primarily works in an office environment and research laboratory from Monday to Friday. The schedule may be altered from time-to-time to meet business or operational needs; may travel to different cities as needed; may also work in a research facility – class 1000 Clean room; adheres to required safety and dress standards (wears a bunny suit); may be exposed to hazardous chemicals, fumes, or vapours and excessive noise from time-to-time while in the wafer manufacturing facility; stands and walks; performs various fine grasping movements, bends, and twists; operates a computer and enters information using a keyboard, operates a telephone, and other office equipment.

Company:

LoMaRe Technologies is a new semiconductor start-up developing emerging non-volatile memory (NVM) technologies with proprietary intellectual property. Headquartered in London, UK, LoMaRe is a spin-off company from world leading institution Imperial College London. Our company's ambition is to commercialise scientific innovation and we are looking to add experienced experts to join our team in China to develop memory technology. Apply to become a part of a future leader in semiconductor chip technology and join a dynamic fast-paced working environment with an ambitious and success-focused team.

To apply, please contact Dr. Andrei Mihai, jobs@lomaretech.com.

职位：纳米蚀刻和特性表征工程师

上司职务：首席技术官（CTO）和高级工艺流程集成/特性表征工程师

地点：常州和苏州， 江苏省

薪金：面议，取决于学历资格和经验

工作类型：全职，永久

职位描述：

在公司 CTO 和高级工艺流程集成/特性表征工程师的指导下，纳米蚀刻和特性表征工程师负责为新技术流程和下一代产品进行原型晶圆的处理和特性表征，包括将薄膜样品蚀刻成纳米/微米级的薄膜功能器件，对原型晶圆进行故障分析以及提出纠正措施。

主要职责：

- 为新器件成功开发并提交蚀刻工艺流程
- 对新开发的流程进行故障分析，并在必要时建议采取纠正措施
- 参与各种其他和复杂性的表征或集成项目；确保它们在规定的时间内完成
- 查看和分析晶圆的表征数据
- 使用聚焦离子束（FIB）/ SEM 工具在交叉结构器件上进行晶圆工艺表征，以识别缺陷并建议纠正措施

- 设计并进行实验以验证工艺流程的耐用性；分析数据并报告结果
- 使用 JMP，MS Visual Basic 或类似软件应用程序分析数据以找出流程变化的根本原因；制作图表或报告，并在小组或团队面前演示
- 与其他团队成员，经理或部门合作
- 遵守所有安全守则和程序
- 履行类似性质或级别的其他职责

工作要求**:**

最低要求：

- 电气工程，材料科学或物理学的硕士学位，和/或同等相关的经验；博士学位优先
- 至少 3 年在半导体工业界/大学中从事制造或工艺流程工程方面的工艺集成或表征工作的实践经验
- 使用各种不同的薄膜构图蚀刻技术的动手经验
- 熟练使用 Microsoft Office 应用程序

知识，技能和能力：

- 对工艺集成和特性表征原理，实践和技术有深入的了解-着重于金属和金属氧化物器件的微/纳米蚀刻
- 磁存储技术/ ReRAM / PCRAM 技术的知识（不是必须，但有加分）— 无尘实验室工艺和特性表征的知识。
- 具有使用 Microsoft Office 应用程序创建电子表格，Word 文档和中英文演示文稿的知识和能力（英文不是必须，但有加分）
- 能够设计实验，分析结果并提出纠正措施
- 能够与各级承包商，顾问，员工和管理层有效地进行中文和英文的口头和书面沟通
- 能够与各级员工和管理层进行有效的合作
- 能够遵守所有安全守则和程序
- 能够运用批判性思维来解决问题，进行根本原因分析并提出改进流程的建议
- 具备分析能力
- 具备组织和时间管理技能
- 具备解决问题和故障排除的技巧
- 灵活且能够优先处理任务

工作环境**:**

从星期一到星期五主要在办公室环境和研究实验室中工作。时间表可能会不时更改，以满足业务或运营需求；可能会根据需要到不同的城市出差。也可能在研究实验室中工作-1000 级无尘室；遵守安全守则的要求和着装标准（穿无尘服）。在晶圆制造工厂中，可能会不时暴露于有害化学物质，烟雾或蒸气以及过多的噪音；站立和行走；进行各种精细的抓握动作，弯曲和扭曲；操作计算机并使用键盘输入信息，操作电话和其他办公设备。

公司**:**

LoMaRe Technologies 是一家新的半导体初创公司，开发具有专有知识产权的新兴非易失性存储器（NVM）技术。 LoMaRe 总部位于英国伦敦，是一家由世界知名大学伦敦帝国理工学院独立出来的公司。公司的目标是将科学创新商业化，我们诚挚地邀请有丰富经验的专家加入在中国的团队，开发内存技术。申请成为半导体芯片技术未来领导者的一员并加入雄心勃勃且以成功为目标的团队和充满活力的快节奏工作环境。

如有意申请，请联系 Andrei Mihai 博士，jobs@lomaretech.com。